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THE LEGAL FRAMEWORK GOVERNING INTEGRATED CIRCUIT LAYOUT DESIGNS IN INDIA

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I. ABSTRACT

The SICLD Act 2000 has been a model of a specialized legal framework that India has established to meet its TRIPS obligations for the protection of the intellectual effort involved in the creation of chip topography. The Indian layout-design scheme is different from the US model which directs the protection towards products of marketed chips. The Indian scheme regards the layout-design as a separate entity. The grant of protection is very much dependent on registration only thus giving the registered owner the exclusive economic rights for a period of ten years. A design to be eligible for registration must be new have some inherent features of distinction and should not have been commercially exploited for more than two years. The Act provides for some exceptions to these private rights in the form of statutory provisions allowing reverse engineering, scientific research, and non-commercial government use. The India Semiconductor Mission (ISM) is anticipated to invigorate local filings and enforcement activities as India's semiconductor consumption is approaching $110 billion by 2030 although the situation has been somewhat stagnant with only two registrations having been recorded by 2016.

II. KEYWORDS

Sui Generis Protection, Inherent Distinctiveness, India Semiconductor Mission (ISM), Reverse Engineering.

III. INTRODUCTION

Life today largely feels seamless because of the sophisticated devices and gadgets that surround us and whenever we go to the market, we are instinctively looking for products that would enhance convenience efficiency and comfort in our daily routines. In a technology driven generation there is always a push to upgrade to the

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"best" devices available where the exclusivity, uniqueness, and high utility of the product become the main factors deciding the consumers." An essential aspect of this situation is to understand the legal system that governs the core of these devices - the semiconductor integrated circuits and their layout designs.

A semiconductor integrated circuit is the central functional unit in a variety of products such as cell phones, wristwatches and washing machines as well as other electronic appliances. These circuits are made based on very detailed plans and the exact composition of transistors and other components on the chip is what is called the "layout design." With the continuous development of technology there is still a very high demand for machines that can process data at a faster rate and are more efficient and this is what pushes the need for layout designs to be smaller in terms of physical size and at the same time be able to perform more complex functions.

The reduction of the dimensions of integrated circuits is a way that less material is needed, and the circuit is taking less space inside any device miniaturization and multifunctionality thus become extremely important commercial goals. The layout designs in the semiconductors are the fruits of human creativity, and they combine the highly specialized skills of a technician with the intellectual effort of a scholar. Their development requires large sums of time expertise and money and consequently an original layout design should be regarded as a valuable piece of intellectual property rather than just a technical drawing.

The reason for unauthorized duplicators to have so much to gain from simply duplicating the layouts at lower prices is that they do not need to go through the long and expensive research and development process. If their copies are sold without the consent of the original creators, the latter side will suffer considerable economic loss due to the decreased demand for their products. To avoid such freeloading to ensure the creators safety in the case of semiconductor integrated circuit layout designs special (sui generis) legal frameworks have been put in place to recognize register and facilitate the enforcement of the rights that the holders have over these designs.

A. Research Objectives

1. To critically examine the statutory framework governing semiconductor integrated circuit layout-designs in India under the Semiconductor Integrated Circuits Layout-Design Act, 2000.
2. To analyse the standards of originality and inherent distinctiveness required for registration of layout-designs.
3. To evaluate the effectiveness of enforcement mechanisms and statutory exceptions under the SICLD Act.
4. To assess the impact of the India Semiconductor Mission on the utilisation of the layout-design registration regime.
5. To identify structural and procedural deficiencies in the present registration and enforcement system.

B. Research Questions

1. Whether the SICLD Act, 2000 provides an effective sui generis framework for protecting semiconductor layout-designs in India.
2. Whether the standards of originality and inherent distinctiveness under the Act are sufficient to distinguish protectable layout-designs from common technical configurations.
3. Whether mandatory registration as a pre-condition for enforcement discourages creators from seeking protection.
4. Whether the criminal-centric enforcement model under the Act is adequate in the absence of strong civil remedies.
5. Whether recent policy initiatives such as the India Semiconductor Mission are likely to increase layout-design registrations and litigation.

C. Research Hypotheses

1. Mandatory registration as a pre-condition for enforcement under the SICLD Act significantly reduces the number of layout-design filings in India.

2. The statutory requirement of inherent distinctiveness imposes a higher threshold than TRIPS standards, thereby limiting registrability of genuine innovations.
3. Absence of explicit civil remedies such as injunctions and damages weakens the deterrent value of the SICLD regime.
4. Government-driven semiconductor initiatives will positively influence the awareness and usage of the SICLD registration framework.

D. Research Methodology

This research adopts a doctrinal and analytical methodology.

Primary sources include the Semiconductor Integrated Circuits Layout-Design Act, 2000, the Semiconductor Integrated Circuits Layout-Design Rules, 2001, TRIPS Agreement Articles 35 to 38, and the IPIC Treaty. Secondary sources include books, journal articles, WIPO materials, government policy documents on the India Semiconductor Mission, and commentaries.

Statutory interpretation is used to analyse provisions relating to originality, inherent distinctiveness, registration, enforcement, and exceptions. Comparative analysis is undertaken with the US Semiconductor Chip Protection Act and Japanese Circuit Layout Rights Act. Policy analysis is used to study the impact of the India Semiconductor Mission on the layout-design ecosystem.

The study is limited to Indian law and international obligations relevant to layout-designs. Empirical data is restricted due to limited reported registrations and litigation.

IV. ANALYSIS

E. From Conception to Codification: The Evolution of the Law

The first legally binding protection for semiconductor chips was initially created in the United States through the Semiconductor Chip Protection Act (SCPA) of 1984[3]. This Act is considered a pioneer as it influenced various legislation and policies all

[3] Semiconductor Chip Protection Act of 1984, 17 USC §§ 901–914.

over the world. Soon after Japan enacted the Japanese Circuit Layout Rights Act (JCLRA) in 1985[4] to provide similar protection to layout designs of integrated circuits within its territory.

After the SCPA and JCLRA, the countries aimed to standardize and globalize the legal protection of semiconductor layout designs and wrought the 1989 Treaty on Intellectual Property in Respect of Integrated Circuits (IPIC Treaty)[5]. The World Intellectual Property Organization (WIPO) a specialized United Nations agency based in Geneva that is dedicated to the promotion and protection of intellectual property rights worldwide served as the forum for the negotiations. The fundamental provisions of the IPIC Treaty were later merged into the Agreement on Trade-Related Aspects of Intellectual Property Rights (TRIPS)[6] mainly in Articles 35 to 38 and therefore, the protection of layout-designs of integrated circuits became an obligation of all the Members of the WTO.

India being a WTO member and TRIPS Agreement signatory, aligned its domestic law with the provisions laid down in the TRIPS Agreement Articles 35-38 through the enactment of the Semiconductor Integrated Circuits Layout-Design (SICLD) Act in 2000.[7] Besides that, the rules for the Semiconductor Integrated Circuits Layout-Design were framed in 2001[8] and the Registrar office as well as the Registry for Semiconductor Integrated Circuits Layout-Design were set up on 1 May 2004. It is interesting to note that most of the core functions granting rights and remedies like those listed in Sections 1(1), 1(2), 2, 3(2), 4, 6-31, 54, 56-92, 95 and 96, were only put into effect from 1 May 2011 in the case of the SICLD Act.

Even though the Semiconductor Integrated Circuits Layout-Design Act was adopted in 2000, and the Registry was formally established in 2004, the fact that the substantive provisions of the Act were not enforced until 1 May 2011 had a considerable negative

[4] Act on the Circuit Layout of a Semiconductor Integrated Circuit (Japan) Act No 43 of 1985.
[5] Treaty on Intellectual Property in Respect of Integrated Circuits (opened for signature 26 May 1989) 28 ILM 1477 (IPIC Treaty).
[6] Agreement on Trade-Related Aspects of Intellectual Property Rights (15 April 1994) 1869 UNTS 299 (TRIPS).
[7] Semiconductor Integrated Circuits Layout-Design Act 2000.
[8] Semiconductor Integrated Circuits Layout-Design Rules 2001.

effect on the practical effectiveness of the Act. The lack of viable rights and remedies are for creators and manufacturers influenced the almost ten-year period, and it discouraged the initial filings and demoralized the industry with the registration system.

They had to set up a separate SICLD system because even the strongest IP protection mechanisms would not be adequate for the purpose of integrated circuits considering the minute and complex nature of chip architecture. The construction of a chip is such that it comprises several disparate parts and features which are then combined to form functional "blocks" and each block in theory can become the subject of a separate patent claim thus making the complete patent specification unwieldy inconvenient and practically impossible for capturing the entire layout-design as such.

The Designs Act 2000 aims at protecting the aesthetic or "ornamental" aspect of articles as opposed to engendering protection for their internal, technical or "functional" side which in the case of integrated circuits is the very aspect that requires protection. Protection as a trade secret under general contract law is also not enough since reverse engineering of a commercially available chip is not only allowed but is also explicitly acknowledged as being in harmony with the IPIC Treaty and TRIPS obligations thus making confidentiality alone an ineffective method for the protection of layout-designs.

F. Protective Mechanisms under the Act

According to the SICLD Act a "Semiconductor Integrated Circuit" means a device comprising transistors other fabric elements and their interconnections either made on the same or the different sides of an insulating material arranged in a one-of-a-kind "layout-design" to achieve an electronic function.[9] The legislation safeguards the "registered proprietor" of a layout-design and enables its use by a "registered user" as per the specified conditions and controls including those indicated in section 25 regarding the permitted use.[10] Under the law the protection depends on registration

[9] Semiconductor Integrated Circuits Layout-Design Act 2000, s 2(r).
[10] ibid s 25.

that is statutory right to sue for infringement or to claim damages is not available to the creator if a layout-design is not registered.

The protection of the layout-design under the law lasts for ten years counting from the date of filing of the registration application or from the date of the first commercial exploitation whichever is earlier be that in India or in any other country once the registration is done.[11]

One of the main reasons for mandatory registration is the fight against "chip piracy" which consists in third parties freely obtaining the latest chip layouts, copying them and then making use of the identical designs for a cheaper price without having to spend a lot on R&D. The consequence of such illegal copying is a significant loss of income for the original designers which is usually the result of a huge investment of money, time, expertise, creativity, and other valuable resources on their part.

Post-registration, the act bestows certain enforceable rights upon the holder such as among others the sole right to use and economically exploit the registered layout-design and to permit (by way of a license) others to do so (registered users). In addition, the notional term of protection is retroactively assigned to the date of the filing or the first commercial exploitation (depending on which of the two is within the two-year filing window).

However, an infringement lawsuit and claims for damages may only be filed from the time of actual registration; for instance, if an application is submitted in May 2022 and registration is granted in August 2023 the protection is considered to be from May 2022 but the right to institute proceedings arises only from August 2023.[12]

The protection offered by the SICLD Act is limited to India in terms of territory but it does not have many restrictions in terms of subject matter because the Act covers the layout-design regardless of whether it has already been included in a finished product.[13] On the other hand, according to the U.S. Semiconductor Chip Protection Act the protection usually revolves around the chip products together with their

[11] ibid s 15.
[12] ibid s 17.
[13] ibid s 18.

incorporation into the articles of commerce while the Indian scheme acknowledges the layout-design as a separate entity that is not dependent on the device in which it is incorporated.

Moreover, the Indian regulation essentially provides two types of cover that is on the one hand it extends to the registered layout-design of the chip proper while on the other hand, it concomitantly covers the product in which such a chip is embedded. Therefore, if a new layout-design "X" is registered, and the wristwatch "Y" in which it is used is marketed in India the protection goes not only to the use of X as a layout-design but also to the illegal commercial exploitation of the products like Y containing the chips embodying X that is in the case of the US protection is focus primarily on the chip product as marketed.[14]

G. Procedural Requirements under the Act

The owner of the layout-design may submit an application to the Registry to have the design registered by following the SICLD Act and Rules requirements. The application must indicate the relevant territorial nexus if the business is located in India the place is considered the appropriate territorial link and if the business is outside India the address for the service specified in the application is considered the territorial reference in India.[15]

Upon the submission of the application the Registrar may demand such changes and alterations as he thinks fit before he proceeds further with the registration and may either grant the application unconditionally or subject to certain conditions or reject it completely. The Registrar is vested with the authority even after provisionally granting his approval to revoke such approval if the layout-design in his opinion falls under any of the statutory grounds of prohibition. This will result in the design not being registered.[16]

The Registrar is bound to advertise the accepted application in the Semiconductor Integrated Circuits Layout-Design Journal within two weeks from the date of

[14] Semiconductor Chip Protection Act of 1984, 17 USC § 902.
[15] ibid s 5.
[16] ibid s 8.

acceptance once an application has been accepted by him. In the case of an application being corrected or amended the Registrar is required to re-advertise it specifying not only the location and the date but also the nature of the corrections or amendments. Any person has the right to submit a notice of opposition according to the prescribed manner within three months from the date of advertisement or re-advertisement (with a possible short extension) by observing the procedure stipulated by the Act and Rules.[17]

The Registrar informs the applicant of the receipt of the notice of opposition. The applicant is given two months to file a counterstatement. If the applicant fails to do so the application is considered abandoned. A copy of the counterstatement is sent to the opponent and after that both parties can submit evidence. If they wish they can also be heard by the Registrar. Not following the prescribed steps may be considered as failure to comply and thus lead to the abandonment of the opposition or application.[18]

Should there be no opposition within the prescribed time, or if any such opposition be raised but decided in favour of the applicant the Registrar will register the layout-design and make an entry of it in the register thus giving effect to the date of the application as the date of registration. A certificate of registration with the seal of the Registry is given to the proprietor.[19] On the contrary if for reasons attributable to the applicant the registration is not done within a period of twelve months from the date of the filing the Registrar, upon giving the due notice may regard the application as abandoned.[20]

V. REGISTRATION FRAMEWORK AND REQUIREMENTS

A. Criteria for Originality under the Semiconductor Integrated Circuits Layout-Design Act 2000

When one talks about layout-designs the case from the beginning is that the individual elements and interconnections used in a semiconductor integrated circuit are basically

[17] ibid s 10; Semiconductor Integrated Circuits Layout-Design Rules 2001, r 25.
[18] Semiconductor Integrated Circuits Layout-Design Act 2000, s 11.
[19] ibid s 13.
[20] ibid s 13(2).

within the technical knowledge domain of layout designers and chip manufacturers. The question that arises is not about the novelty of each separate element but whether the overall combination and arrangement of these elements taken as a whole is original or different and shows the creator's own intellectual effort.

According to the SICLD regime a layout-design is regarded as "original" when it is the outcome of the creator's own intellectual initiatives and is not common knowledge to other layout-design creators and manufacturers of semiconductor integrated circuits at the time of its production.[21] The design is considered original even if the components (elements and interconnections) are common provided that the combination when looked at as a whole is the result of the creator's intellectual labour and yields a new overall configuration.[22]

The layout-design which is to be given a patent must have an overall configuration that is different from that of the already existing layout-designs that is the design should have different features when compared with what is already registered or being used. In comparison with copyright law where the level of "originality" is generally lower and patent law where the "novelty" requirement is significantly more rigorous the SICLD Act stands in between with its own specific standards of originality and distinctiveness.[23]

An elite characteristic of Indian semiconductor law is the explicit stipulation of "inherent distinctiveness" which is not there in IPIC Treaty as well as the TRIPS Agreement.[24] The Act and the comments on it suggest two main criteria for determining inherent distinctiveness the first one is that the functions of the layout-design should be new or different from those of the existing layout-designs and the second is that one or more elements or compounds used in the layout-design should be the newest in the relevant industry that is the use of newly developed alloys.[25]

[21] ibid s 7(1)(a).
[22] ibid s 7(2).
[23] ibid s 7(1)(b).
[24] ibid s 7.
[25] TRIPS, art 35 (referencing IPIC Treaty, art 3).

B. Requirements for Registration of Integrated Circuit Layout Designs

Section 7 of the SICLD Act defines the circumstances in which a layout-design cannot be registered, so knowing its aspects is vital at the registration level. The article refers to four cumulative grounds of denial of a layout-design in the registry each of these in combination prohibits a layout-design from being listed on the register.

If a layout-design is not "original" that, is it is not the creator's own intellectual product or is generally known to layout-design creators and semiconductor manufacturers it will not be registered. The design has to be evaluated as a whole if the entire combination does not show enough intellectual effort to make it original then it is considered that the design contravenes section 7 even if the individual elements and interconnections are known. A design that has been commercially exploited anywhere in India or a convention country cannot have its layout-design registered. The provision clearly aims to protect the designs which are not fully released in the market.

Nevertheless, there is a provision for a temporary exception if the design has been commercially exploited for two years at the most from the date of filing the application for registration (in India or a convention country) it is "deemed" not to have been commercially exploited for the purposes of section 7 and therefore the applicant is not disqualified on that ground. Section 7 talks about "commercial exploitation" the main focus being the commercial character of the activity rather than whether a direct monetary payment has been received. Therefore, a layout-design might be regarded as one that has been exploited commercially even if such exploitation is just a part of a larger commercial plan or business use and there is no immediate link to a specific monetary gain.

The third point of prohibiting a design is that the layout-design is not "inherently distinctive" in other words it does not have a sufficiently distinctive configuration of elements and interconnections. The fourth one is that the design is not inherently capable of being distinguished from any other registered layout-design that is when viewed as a whole the content is too similar to what is already on the register to be valid as a separate, protectable layout-design.

C. Transfer of Integrated Circuit Layout Design Rights in India

Chapter V of the SICLD Act details the various methods by which rights of registered layout-design may be handed over to another party through assignment or transmission.[26] The Act illustrates the differences between these two types of transfer in relation to a registered layout-design and emphasizes that any transaction of this kind has to be done according to the formalities specified in this chapter.[27] It must be an instrument in writing any assignment or transmission of a registered layout-design.[28] The transfer may take place either together with the goodwill of the business or without this goodwill. In the case where an assignment occurs without goodwill the assignee within six months from the date of the assignment (or within a further period not exceeding three additional months, if allowed) must seek the Registrar's directions as to the advertisement of the assignment and thereafter proceed with advertising it in the manner prescribed.

Pursuant to section 23, a person who through an assignment or transmission becomes entitled to a registered layout-design is obliged to apply to the Registrar in the prescribed form to have his or her ownership recorded in the register. Upon confirmation of the assignee's or transferee's entitlement the Registrar records the details of the assignment or transmission in the register thus granting the new owner formal recognition of the layout-design rights under the Act.[29]

D. Concept of a Registered User of a Layout Design

Section 24 allows a person other than the registered owner of a topography to be regarded as its "registered user". Section 25 then lays down the steps to be followed to get such a user registered. Joint application and required documents. Being registered as a user of a layout-design is a situation that requires a joint written application by the registered owner and the user to be registered, which has to be submitted before the Registrar in the prescribed manner and form.

[26] ibid s 19.
[27] ibid s 20.
[28] ibid s 22.
[29] ibid s 23(2).

This application should also be accompanied by-An agreement in writing between the owner and the proposed registered user specifying the vendor's rights of use of the topography and an affidavit of the registered owner (or an authorized person) stating the current or future relationship between the owner and the user the level of control over the permitted use the number of the users registered any clauses limitations and territorial scope of use and the term of the permitted use. After these conditions have been met the Registrar records the person as a registered user and if there are other registered users sends a notice to them.[30]

Section 28 authorizes a registered user subject to any subsisting agreement with the proprietor to bring a complaint to the competent criminal court for infringement in the registered user's own name as if he or she were the registered proprietor. Section 26 allows the Registrar to revoke a user registration on a number of grounds including significant misrepresentation or failure to disclose information that would have resulted in refusal change of circumstances making the registration no longer valid conflict with pre-existing contractual rights, breach of agreed terms (for instance relating to topographical dimensions) termination of the underlying layout-design.

Section 29 specifically states that the Act does not give a registered user any assignable or transferrable right to use the layout-design. The explanation provides that there is no "assignment" or "transmission" in cases where-An individual registered user forms a partnership, and the firm uses the topography while that person remains a partner or A company which is a registered user is reconstituted and the partner who was the registered user continues as a partner of the reconstituted company.

Every proceeding under Chapter VII (rectification and correction of the register) necessitates as per the Act the inclusion of each registered user of the layout-design as a party even if the registered user is not the moving party. A registered user so impleaded is not liable for costs unless he or she appears and takes part in the proceedings and this position also applies at the appellate stage.[31]

[30] Semiconductor Integrated Circuits Layout-Design Act 2000, ss 24–25.
[31] ibid s 28.

E. Scope and Application of Statutory Exceptions

The SICLD Act 2000 sets out different provisions that in some cases treat the acts as lawful when they would have been otherwise considered illegal under a registered layout-design. The exceptions that are carved out by the law serve to balance the proprietary interests of chip designers with the concerns of the public and competition. One such exception is the reproduction of a registered layout-design for the limited purposes of scientific evaluation analysis, research or teaching which is not considered an infringement.

In particular the Act provides a small space for reverse engineering within the umbrella of scientific use. Accordingly, a person may study and analyse an existing layout-design in order to understand its operation or to create an improved or a competing design especially when this leads to pro-competitive objectives and prevents anti-competitive conduct in the semiconductor sector.[32]

Apart from these, the Act allows use by the Government and third parties authorized by the Government in certain circumstances. Such use without the proprietor's prior consent is permitted only if it is necessary for non-commercial public purposes such as national emergency situations of extreme public urgency needs of the public interest or the removal of anti-competitive practices and the registered proprietor is paid the corresponding remuneration of course.[33]

The rationale behind these exceptions is that they represent an intention of the legislator to protect a significant private investment in layout-designs and at the same time to encourage research the spread of technical knowledge and fair competition in the semiconductor industry. By protecting scientific uses and certain public-interest uses the SICLD framework is designed to keep innovation and development going in the long term rather than to allow exclusive rights to become a barrier to technological progress.

[32] ibid s 18(2)(b).
[33] ibid s 51.

F. Enforcement, Liabilities, and Penal Sanctions for Layout Design Infringement

Chapter IX of the SICLD Act outlines the criminal offences and associated penalties that are applicable to violations of registered layout-designs. Penal and forfeiture remedies dominate the scene rather than civil damages.[34] Any person who in any way violates a layout-design as per Section 18 is liable to imprisonment for a term which may extend to three years or to a fine of not less than fifty thousand rupees and up to ten lakh rupees or to both.

As per Section 57 the person who is found to be misrepresenting an unregistered layout-design as a registered one in the first place will be punished by imprisonment up to six months or with a fine up to fifty thousand rupees or with both. There is also a provision for separate punishment in case a person wrongly refers to a business as being officially associated with the Semiconductor Integrated Circuits Layout-Design Registry.

The Act provides a shield for "innocent buyers" of infringing chips who after learning of the infringement, pay a reasonable royalty to the registered proprietor such buyers are then granted immunity from further liability. It is worth pointing out that the SICLD system is silent about the availability of civil remedies such as injunctions accounts of profits or compensatory damages rather the main monetary remedy for infringement is the payment of royalty to the proprietor[35] which can be either negotiated or determined as per the Act.

According to section 60, if a person is found guilty of an offence under section 56 (penalty for infringement of layout-design) the court may decide that all goods and things that were used for the commission of the offence or are related to it be taken away from the person and handed over to the Government. Besides that, the court may order that the seized goods be destroyed or given to someone else in any other way that it deems appropriate thus making sure that both the infringing semiconductor products and the related materials are no longer available for sale.

[34] ibid ss 56–58.
[35] ibid s 18(3).

G. Contemporary Developments and Emerging Trends in India

India passed a law specifically for the layout design of semiconductors in 2000 but the main provisions of the law only became operational much later and the practical application of the law has been very limited so far. Over the same period India's semiconductor consumption and policy ambition have risen dramatically resulting in a significant push under the India Semiconductor Mission and related programmes up to 2025.[36]

While the Semiconductor Integrated Circuits Layout-Design Act was enacted in 2000 several significant sections were only enforced years later and the Registry had not received any layout-design applications until around October 2014. It is reported that the Registry has so far only issued two certificates of registration - one to Bharat Electronics Ltd. (BEL) in January 2015 and the other to the Indian Space Research Organisation (ISRO) in May 2016 which indicates that the practical area of this IP right is very limited.

Based on industry figures and policy analyses India's semiconductor consumption has been rapidly increasing and is forecasted to be around 80-100 billion USD by the mid-2020s and close to 108-110 billion USD by 2030 which may represent almost a 10% share of the total global demand. Nevertheless, India continues to be a major importer of chips whereas the most advanced manufacturing at sub 10 nm nodes is only available to a handful of economies such as Taiwan and South Korea.

The Union Cabinet gave the green light to the India Semiconductor Mission (ISM) in 2021 with an approximate total outlay of ₹76,000 crore aimed at creating semiconductor and display industries with the inclusion of attractive fiscal incentives for fabs and packaging or assembly units. Ten semiconductor projects under ISM with a total investment of about ₹1.6 lakh crore spread over several states have been approved according to government statements indicating the commencement of the local manufacturing capacity build-up by 2025.[37]

[36] MeitY, 'India Semiconductor Mission' (Government of India 2021).
[37] MeitY, 'Annual Report 2024-25' (Government of India 2025).

One of the main projects is that of Micron Technology which refers to the ATMP/OSAT plant in Sanand, Gujarat where the investment is more than ₹22,000 crore and the primary objective is to complete assembly and testing of DRAM and NAND products in India. Simultaneously, proposals related to Tata Electronics (Gujarat, Dholera fab) reshaped initiatives of Foxconn after the Vedanta-Foxconn joint venture cancellation and ongoing design as well as specialized semiconductor activities at ISRO and defence connected entities areas are being talked about.

The Indian government has leveraged the Semicon India conference series initiated in 2022 and carried on annually as an opportunity to attract global majors and reveal India's policy framework infrastructure amenities and talent pool. All these occasions together with ISM incentives have resulted in some companies such as Micron, Foxconn-group entities, Vedanta's reoriented ventures, AMD and others pledging or showing interest although many of the projects are still at their infancy or transitional phase.

VI. SUGGESTIONS AND RECOMMENDATIONS

1. **Introduction of Civil Remedies**: The SICLD Act should be amended to expressly provide civil remedies such as injunctions, compensatory damages, and accounts of profits to strengthen enforcement.
2. **Simplification of Registration Procedure**: The Registry should introduce fast-track and online filing systems with reduced fees for startups and academic institutions.
3. **Awareness and Capacity Building**: Government agencies under ISM should conduct training programmes and workshops to educate chip designers and fabs about layout-design protection.
4. **Revisiting the Inherent Distinctiveness Standard**: The standard should be aligned more closely with TRIPS to avoid excessive rejection of genuine innovations.
5. **Strengthening Institutional Infrastructure**: Dedicated benches or specialised IP courts should be authorised to handle SICLD disputes for faster adjudication.

VII. CONCLUSION

Indian law with respect to integrated circuits and semiconductors principally the SICLD Act 2000 is well equipped structurally and comprises lots of unique elements that are aimed at the protection of the layout-designs creators after their registration. The law accords a ten-year term of protection to registered layout-designs and couples this protection with a prior registration thereby delineating a clear legal framework of rights and their enforcement. The establishment of protection as a requirement of registration is aimed at curtailing subsequent disputes over "prior use" or competing claims to the same layout-design since the register itself operates as the authoritative record of rights.

From the substantive angle the law confines its protection only to those designs that are original inherently distinctive and can be differentiated from the ones already registered thus directing the protection to real non-trivial innovations in chip layout topographies. Simultaneously, the law provides for public interest measures for example limited government and authorised third-party use and research and reverse engineering defence that permit compulsory or non-voluntary use in situations of emergencies, welfare objectives and procompetitive purposes. Though the statutory framework is relatively strong the SICLD regime has been poorly utilized official data and commentary show that only a few layout-designs have ever been registered and that for many years after the enactment of the law the Registry barely received any applications.

In line with that, as per the report's litigations under the SICLD Act are very few and hence there are only limited instances where its provisions have been directly challenged before Indian courts which in turn limits the formation of judicial doctrine on the issues of infringement exceptions and royalty valuation.

The low usage of the registration system is an indication of and a factor that contributes to the present situation of weak domestic innovation and commercialization in the area of semiconductor layout-designs in which unregistered designs not only remain unreported but also do not become the subject of disputes which would result in IP litigation. Nevertheless, the India Semiconductor Mission

along with the incentive schemes has been attracting substantial investments of fabs, ATMP/OSAT facilities and design ecosystems and therefore the commentators are optimistic that there will be a gradual increase in layout-design registrations and as a consequence the onset of SICLD related disputes and enforcement actions scheduled for the future years.

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